UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/880,734	06/12/2001	Andrew Crosland	015114-053500US	4950

26059 7590 01/23/2007

TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/880,734	CROSLAND ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-15,44 and 46-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7 and 10-15* is/are allowed.

6)☒ Claim(s) *44,46-50 and 52-54* is/are rejected.

7)☒ Claim(s) *51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 14, 2006 has been entered.

2. Claims 1-7, 10-15, 44, 46-54 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 44, 46-50, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokouchi, in view of Van de Steeg and May.

5. In re claim 44, Yokouchi discloses a method of operating a programmable logic integrated circuit [cpu] comprising [fig.2; col.1, ll.36-54]:

- Clocking a watchdog timer circuit on the programmable logic integrated circuit [cpu, mpu] [col.1, ll.6-14] to advance a count register that is part of the watchdog timer circuit [enable the counter for free-running counting].
- Loading a first magic value [data e1H] into a reload register [inherently, some kind of reload register in the broadest interpretation is needed to secure the value] that is a part of

the watchdog timer circuit, which resets [initializes] the count register to an initial value, wherein the first magic value configures the watchdog timer circuit to respond to a second magic value [1eH] that is different from the first magic value, wherein the second magic value when loaded into the reload register configures the watchdog timer circuit to respond to a third magic value [e1H] that is different from the second magic value [col.1, ll.36-50].

- After loading the first magic value, loading the second magic value [data 1eH] into the reload register, which causes the count register to reset the initial value [col.1, ll.36-50; combination of data written for resetting].
- After loading the first magic value into the reload register, loading a value other than the second magic value or the third magic value into the reload register, which causes the watchdog timer circuit to generate a triggered signal [carry signal] [col.1, ll.48-54; incorrect combination written will cause reset].
- Receiving the triggered signal in a reset logic block [reset receiving circuit 5] on the programmable logic integrated circuit, which causes a reloading of configuration data [from address 0] into the programmable logic integrated circuit [col.1, ll.36-54].

6. Yokouchi did not discuss the details of loading configuration data and did not disclose explicitly integrating the circuit components on a single die.

7. Steeg discloses a method of operating a programmable logic integrated circuit [plc 29, 37] comprising:

- Receiving a triggered signal [reset/clear] in a reset logic block [fault logic circuit], which causes a reloading of configuration data from an external source [prom 25] into the programmable logic integrated circuit [col.3, ll.28-53; col.8, ll.49-59; col.9, ll.54].

8. May discloses a method of operating a programmable logic integrated circuit wherein the programmable logic integrated circuit and another circuit [e.g., watchdog timer] are disposed on the same die [col.40, ll.1-41, l.61 col.41, l.6; col.42, l.43 – col.43, l.3; circuit components including the isolation interface integrated on a single die].

9. It would have been obvious to one of ordinary skill in the art, having the teachings of May, Steeg and Yokouchi before him at the time the invention was made, to include the external source for configuration data taught by Steeg for the programmable logic integrated circuit disclosed by Yokouchi as the external source for configuration data taught by Steeg is very well known for use with the programmable logic integrated circuit of Yokouchi; and to integrate the circuit components of Yokouchi [e.g., watchdog timer, CPU/MPU] onto a single die as taught by May in order to minimize the area required for integrated components [May: col.39, ll.53-67]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to have a software re-configurable system that would be more flexible in adapting to changes in operations [Steeg: col.2, ll.2-29] and counter against problems associated with external noise, aging, etc. [Yokouchi: col.1, ll.6-13; May: col.39, ll.53-67].

10. As to claim 46, Steeg discloses each and every limitation of the claim as discussed above in reference to claim 10.

11. As to claim 47, Steeg discloses the method wherein the watchdog timer circuit [60] is located in an embedded processor portion [plc 29] and the reset logic block [fault logic 78] is

located in a programmable logic portion [plc 37] of the programmable logic integrated circuit [fig.2, 4-5].

12. As to claim 48, Yokouchi discloses the method comprising allowing the count register that is a part of the watchdog timer circuit to advance to a final value [fixed time; e.g., 16 ms] before the first or second magic values are loaded, which causes the watchdog timer circuit to generate the triggered signal [col.1, ll.36-54].

13. As to claim 49, Yokouchi discloses the method wherein the initial value is 0 [col.1, ll.36-47].

14. As to claim 50, the Examiner had taken Official Notice that it is well known in the art to have an initial value that is a value other than 0.

15. As to claim 53, see discussion above in reference to claim 14.

16. Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over May, Yokouchi and Steeg as applied to claims 48 above, and further in view of Muller, US Patent 6298360.

17. In re claim 52, May, Yokouchi and Steeg disclose each and every limitation of the claim as discussed above in reference to claim 48. May, Yokouchi and Steeg did not disclose explicitly that the final value is user-selectable.

18. Muller discloses a method comprising a value that is user-selectable [col.6, ll.30-46].

19. It would have been obvious to one of ordinary skill in the art, having the teachings of Muller, May, Yokouchi and Steeg before him at the time the invention was made, to modify the programmable logic integrated circuit taught by May, Yokouchi and Steeg to include the teachings of Muller, in order to obtain the final value that is user-selectable. One of ordinary skill

in the art would have been motivated to make such a combination as it provides a way to initialize a timer [Muller: col.6, ll.30-46].

20. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over May, Yokouchi and Steeg as applied to claims 44 above, and further in view of Laiho et al., US Patent 6754830, hereinafter Laiho.

21. In re claim 54, May, Yokouchi and Steeg disclose each and every limitation of the claim as discussed above in reference to claim 44. May, Yokouchi and Steeg did not discuss the details of a debug mode.

22. Laiho discloses a method wherein in a debug mode, the count register [watchdog register] does not advance [col.4, ll.27-41].

23. It would have been obvious to one of ordinary skill in the art, having the teachings of Laiho, May, Yokouchi and Steeg before him at the time the invention was made, to modify the programmable logic integrated circuit taught by May, Yokouchi and Steeg to include the teachings of Laiho, in order to not advance the count register in debug mode. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to perform debugging [Laiho: col.4, ll.27-41].

Allowable Subject Matter

24. Claims 1-7, 10-15 are allowed.

25. Claim 51 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

26. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Response to Arguments

27. Applicant's arguments dated November 14, 2006 have been considered but are moot in view of the new ground(s) of rejection.

28. Examiner iterates that integrating watchdog timers – just another circuitry, is well known and well within knowledge of one with ordinary skill in the art.

29. Regarding Applicant's argument about Yokouchi teaching against "writing two static values within a specified time in order for the reset to occur", Examiner submits that Yokouchi was used to explicitly identify a very well known method involving watchdog timers "writing two static values within a specified time in order for the reset to occur".

30. Applicant's arguments about Yokouchi's specific embodiments were not cited in the rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
January 11, 2007

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
1/17/06